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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,255	10/22/2003	Terry Lines	100-14310 (P04927-C1)	9418
33402	7590	07/12/2005	EXAMINER	
LAW OFFICES OF MARK C. PICKERING			LEE, EUGENE	
P.O. BOX 300			ART UNIT	
PETALUMA, CA 94953			PAPER NUMBER	

2815

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/692,255

Applicant(s)

LINES, TERRY

Examiner

Eugene Lee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 13 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 3-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 3-9 is/are allowed.
- 6) ☒ Claim(s) 10-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 October 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/13/05 has been entered.

### ***Drawings***

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the no region of the first conductivity type with a dopant concentration substantially greater than the dopant concentration of the second semiconductor region lying between the second source and drain regions (claim 10) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

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renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 10 thru 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not describe the second channel having ... the first conductivity type, no region of the first conductivity type with a dopant concentration substantially greater than the dopant concentration of the second semiconductor region lying between the second source and drain regions.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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6. Claims 10 thru 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what the applicant is stating in the limitation “no region of the first conductivity type with a dopant concentration substantially greater than the dopant concentration of the second semiconductor region lying between the second source and drain regions.”

*Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Insofar as definite, claims 10 thru 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein 4,205,330 in view of Takagi 4,003,071. Klein discloses (see, for example, Fig \_4) a MOSFET circuit (semiconductor circuit) comprising a depletion mode device (first transistor) wherein the depletion mode device comprises a first semiconductor region, source 37, drain 38, region (first channel) 30a, first gate oxide 29a, and gate 34; an enhancement device (second transistor) wherein the enhancement device comprises a p-type region (second semiconductor region) 25, N+ region (source) 35, N+ region (drain) 36, region (second channel) 30, second gate oxide 29, and gate 32. The length of region 30a is shorter than the region 30. Klein does not disclose the gate being spaced apart from the first source region. However, Takagi discloses (see, for example, FIG. 1J) Takagi discloses (see, for example, FIG. 5) a

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semiconductor device comprising a depletion mode transistor 43 wherein the depletion mode transistor comprises a gate 47 spaced apart from a source 49. This structural arrangement is one of many arrangements used to form a depletion mode transistor. It would have been obvious to one of ordinary skill in the art at the time of invention to have the gate being spaced apart from the first source region in order to separately apply a voltage to the source independent of the gate.

Regarding claim 11, Klein does not disclose the layer of first gate oxide having a first thickness, and the layer of second gate oxide having a second thickness that is substantially greater than the layer of first gate oxide. However, Takagi discloses (see, for example, FIG. 6A) a semiconductor device comprising a depletion mode transistor 63 with a gate insulating film 66, and an enhancement-type transistor 62 with a gate insulating film 65. The thickness of the gate insulating film 66 of the depletion mode transistor is substantially less than the thickness of the gate insulating layer 65 of the enhancement mode transistor. In column 8, lines 17-34, Takagi discloses that gate insulating layer of the depletion mode transistor permits the formation of the impurity diffused layer whereas the gate insulating layer of the enhancement mode transistor prevents it. Therefore, it would have been obvious to one of ordinary skill in the art to have the thickness of the layer of first gate oxide being substantially less than the thickness of the layer of second gate oxide in order to only form the layers necessary in the formation of an enhancement and depletion mode transistor, and to save in manufacturing steps.

Regarding the limitation "the first transistor conducting more than leakage current when the gate, the source, and the first semiconductor region are connected to a same potential (which is a depletion device according to applicant's specification on page 1)" and the limitation "the

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second transistor being substantially non-conductive when the gate of the second transistor, the source of the second transistor, and the second semiconductor region are connected to a same potential (enhancement device)", see, for example, column 4, lines 10-11 wherein Klein discloses the depletion mode device with region 30a and the enhancement device with region 30.

***Allowable Subject Matter***

9. Claims 3 thru 9 are allowed. The following is a statement of reasons for the indication of allowable subject matter: The references of record, either singularly or in combination, do not teach or suggest at least a semiconductor circuit comprising: a third transistor formed in the semiconductor material, the third transistor having a third channel and a layer of third gate oxide formed over the third channel, the third channel having a third channel length and a third dopant concentration, the layer of third gate oxide having a thickness, the third transistor being substantially non-conductive when zero volts are applied to the gate, the thickness of the layer of third gate oxide being substantially equal to the thickness of the layer of first gate oxide.

***Response to Arguments***

10. Applicant's arguments with respect to claims 3-14 have been considered but are moot in view of the new ground(s) of rejection.

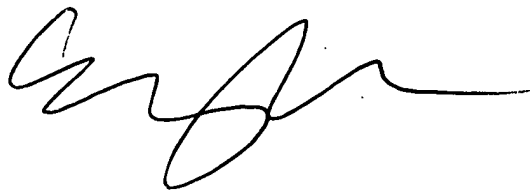
### INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee  
July 7, 2005

A handwritten signature in black ink, appearing to be 'Eugene Lee', with a long horizontal flourish extending to the right.